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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,656	07/03/2003	Anthony Zalenski	1970-0005C	2953

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EXAMINER	
JAMAL, ALEXANDER	
ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,656	ZALENSKI ET AL.	
	Examiner	Art Unit	
	ALEXANDER JAMAL	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,11-15,17-19,21-23,44,46-50 and 53-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Based upon the submitted amendment, the examiner notes that claims 1,2,4-7,11-15,17-19,21,44,46-50,53-55 have been amended, claim 56 has been added, and claims 3,8-10,16,20,24-43,45,51,52 are cancelled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1-55** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The independent claims recite a first memory and a second memory. It is not clear what defines a memory or how to distinguish one memory from another. For the purpose of examination the examiner assumes each address location in a memory may be read as a separate memory.

As per **claims 48,49,** the claims recite that the first memory **includes** a flash device, and the second memory **includes** a RAM device. It is again not clear what separates one memory from another as applicant is already stating in the claims that a

'first memory device' may comprise more than just a single flash memory device or Ram memory device. It is not clear what defines a 'memory'.

As per **claim 51,** it is not clear what exactly defines 'template state data' as such it is not clear how one template state data is determined at least partially by another template state data. For the purpose of examination the examiner reads the separate templates (finite state machines) of Moon as being interdependent since they are both implemented by the same processor in the same system.

As per **claims 14-23,46,53-55,** it is not clear how the disclosed invention defines a called party responding or not responding to a message. How does the system differentiate between an actual person responding and the voice of a voicemail answering system ?

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-** rejected under 35 U.S.C. 103(a) as being unpatentable over Trachewsky (US 20040017794 A1) and further in view of Moon (US 20020161907 A1).

As per **claims 1,56,** Trachewsky discloses a gateway device that supports multiple protocols (abstract) but does not disclose the specific implementation of the gateway using a virtual machine to implement the disclosed functions.

Moon discloses using a finite state machine implemented in a processor in order to implement an adaptable, multi-protocol system (ABSTRACT, para. 92). It would have been obvious to one skilled in the art at the time of this application to use a well known processor implementation as a matter of design choice.

Trachewsky discloses the use of multiple protocols. Each protocol inherently comprises software/firmware templates to control the gateway according to the desired protocol. The device comprises a processor to control the digital hardware nad inplement the programmed instructions. The system (virtual machine) must inherently store and read the various protocol in order to retrieve and process them during the selection process. This would inherently comprise the CPU steps of claim 1. Further, the system must inherently send 'state data' in order properly determine if the memory has been correctly read or written to (the state data could be clocking or bus interface information for example). The system is a digital system implemented on a processor with memory and as such requires software and firmware in order to implement the disclosed protocol selection function. Each protocol has a selectable state and a 'template' in order to interface with the rest of the system. As such there is one 'template' associated with each protocol. Each protocol and virtual machine state and instruction requires a separate memory area (first, second third ect. memory). Additionally (para. 37) it is disclosed that

the processor can be implemented with a plurality of memory devices (such as flash and ram. Each memory location will have only one piece of stored information (such as a virtual machine instruction as taught by moon) at a time.

As per **claims 7,22,23,** they are rejected as per the claim 1 rejection.

As per **claims 2,6,15,19,** Trachewsky discloses multiple protocols, but does not specify the group of protocols consisting of (DHCP,H.323,STUN, and SIP).

It would have been obvious to one skilled in the art at the time of this application to use any well known protocols as a matter of design choice.

As per **claim 5,18,** after a first protocol is attempted, if it is not successful another (second) protocol will be activated in the same manner as the first (claim 1 rejection). Each protocol and associated instructions for interfacing with the system by that particular protocol is considered a separate template, and separate set of virtual machine instructions.

As per **claims 11-13,** it would have been obvious to use a well known connection means (such as a parallel or serial bus) in order for the processor and ram to communicate.

As per **claims 4,17,21,** they are rejected as per claim 3 rejection. The system inherently comprises I/O ports for the purpose of each component communicating to each other.

As per **claim 44,52,** Moon discloses (para. 103) a configuration table and exception table for each finite state machine (or 'template' as claimed by applicant) where the state and behavior of the template may be changed. The tables require separate memory to function (a second memory). The 'updated' template state data must be read from a memory in order to be acted upon.

As per **claim 45,** since the behavior of the template will change, it will communicate different information to the processor (subsequent virtual machine instructions) based on any changed to the template.

As per **claim 46**, it would have been obvious to one skilled in the art that a signaling bus to a 'memory' could have less lines than memory-address storage places in said memory. As such the data transferred to the memory over said bus would have to be performed sequentially (at different times).

As per **claim 47,** as per the rejections above it is not clear how to exactly define a 'memory'. However, the examiner contends that each memory device would be chosen as a matter of design choice (storage capacity versus cost/space). It would have been obvious to design the memories to be the desired size per the particular application.

As per **claims 48,49,** moon discloses a Flash and RAM used with the processor used to implement the finite state machine.

As per **claim 50,** the system can select any number of protocols to be used. This would require a request to implement a protocol (such as a second protocol), memory to communicate/store the request. Moon discloses (para. 103) a configuration table and

exception table for each finite state machine (the 'template' is the inherent interface between the finite state machine and the microprocessor) where the state and behavior of the template may be changed. The tables require separate memory to function (a second memory).

As per **claim 51,54,** Moon discloses the interdependent templates as per the 112 rejection above. Additionally, a first protocol is attempted, and based on the results of that protocol initialization, a second protocol may be initialized.

As per **claim 53,55,** the examiner reads the address where each 'virtual machine instruction' is stored as a separate memory. As such they will not be stored concurrently.

Response to Arguments

1. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

As per applicant's responses to the 112 rejections, the examiner notes that it is still unclear as to how to differentiate one memory from another, and it still is not clear what defines a single virtual machine instruction.

As per applicant's arguments concerning the single virtual machine instruction, it is not clear how a single virtual machine instruction is defined.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 571-272-7498, and whose email address is alexander.jamal@uspto.gov

The examiner can usually be reached on M-F 8AM-5PM.
If attempts to reach the examiner by telephone or email are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 571-272-7499.

The fax phone numbers for the organization where this application or proceeding is assigned are **571-273-8300** for regular communications and **571-273-8300** for After Final communications.

/Alexander Jamal/

Primary Examiner, Art Unit 2614

Examiner Alexander Jamal

July 21, 2009